WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

a cell-array region formed in the substrate and having a plurality of dynamic memory cells each of which includes a capacitor and a transfer transistor having a gate electrode, a drain region and a source region;

first side insulating films formed on sides of the gate electrode of each transfer transistor;

a peripheral region formed in the substrate, located adjacent to the cell-array region and including a transistor which has a gate electrode, a drain region and a source region; and

a first contact which is self-aligned in the cell-array region, which is provided between the gate electrodes of any two adjacent transfer transistors, with two first side insulating films interposed between the first contact and the adjacent transfer transistors, and which has first and second ends, the first end directly contacting the drain regions of the adjacent transfer transistors.

2. The device according to claim 1, wherein a silicide layer is formed by means of salicide process on a word line which includes the gate electrode and the second end of the first contact.

3. The device according to claim 2, wherein the

first side insulating films have tops which lie at a level higher than the surface of the silicide layer provided on the gate electrode.

4. The device according to claim 2, wherein the surface of the silicide layer provided on the upper surface of the first contact lies at a level higher than the surface of the silicide layer provided on the word line.

5. The device according to claim 4, wherein the silicide layer on the upper surface of the word line and the silicide layer on the upper surface of the first contact are of the same material.

6. The device according to claim 4, wherein second side insulating films are formed on the sides of the gate electrode of the transistor provided in the peripheral region and have tops which lie at a level higher than the surface of the gate electrode of the transistor.

7. The device according to claim 1, wherein the capacitor is a buried-strap type trench capacitor.

8. The device according to claim 1, further comprising a second contact which is self-aligned in the cell-array region, which is provided between the gate electrodes of any two adjacent transfer transistors, with two first side insulating films interposed between the second contact and the adjacent transfer transistors, and which has first and second

ends, the first end directly contacting the source regions of the adjacent transfer transistors.

9. The device according to claim 8, wherein the capacitor is a surface-strap type trench capacitor which has a storage node that is connected to the source region by the second contact.

10. The device according to claim 8, wherein the capacitor is a stack capacitor which is formed on the second contact, is located above the bit line and constituting a capacitor-over bit line type stack cell.

11. The device according to claim 8, wherein the capacitor is a stack capacitor which is formed on the second contact, is located below the bit line and constitutes a capacitor-under bit line type stack cell.

12. The device according to claim 8, wherein each of the dynamic memory cells is formed in the silicon substrate, comprises an FIN-type transistor and a trench capacitor and constitutes a surface-strap type trench cell which has a storage node connected to the source region by the second contact.

13. A method of manufacturing a semiconductor device, comprising:

forming in a substrate a plurality of gate structures in surfaces of a cell-array region and a peripheral region of the substrate, each gate structure having a gate electrode and a cap insulating film formed on the gate electrode;

forming first side insulating films on the sides of each gate structure;

forming drain regions and source regions in the substrate, in self-alignment with the gate structures, respectively;

burying gaps between the gate structures with first insulating film;

planarizing a surface of the first insulating film;

removing one first insulating film between two adjacent gate structures provided in the cell-array region, for making a first hole and exposing one drain region provided in the cell-array region; and

forming a conductive film in the first hole, the conductive film being used as a first contact which contacts the drain region and which has a top lying at almost the same level as the surface of the first side insulating films.

14. The method according to claim 13, further comprising:

removing the cap insulating film, for exposing the gate electrodes;

forming silicide layers on the gate electrodes, drain regions and source regions and first contact;

forming a second insulating film on the entire surface of the resultant structure;

planarizing a surface of the second insulating

film;

making a plurality of second holes in the second insulating film, for exposing the gate electrodes, drain regions, source regions and exposing the silicide layers formed on the gate electrodes; and

forming wire layers in the second holes, the wire layers being connected to the silicide layers.

15. The method according to claim 13, further comprising:

removing another first insulating film from the cell-array region at the same time the first hole is made, for making a third hole that exposes the source region; and

forming a conductive film in the third hole, the conductive film being used as a second contact which contacts the source region and which has a top lying at almost the same level as the surface of the first side insulating films.

16. The method according to claim 15, further comprising:

forming trench capacitors in the cell-array region before the gate structures are formed.

17. The method according to claim 15, further comprising:

forming a stack capacitor above the first contact.

18. The method according to claim 17, further comprising:

forming a bit line above the stack capacitor.

19. The method according to claim 17, further comprising:

forming a bit line below the stack capacitor before the stack capacitor is formed.

20. The method according to claim 17, wherein an active region having a projection is formed in the substrate, and two adjacent gate electrodes are formed on the sides of the projection.